

Notice of References Cited	Application/Control No. 10/051,276	Applicant(s)/Patent Under Reexamination SHIMBO ET AL.	
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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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	B	US-2002/0010730	01-2002	Blaker, David M.	708/491
	C	US-2002/0120658	08-2002	Chen et al.	708/491
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	L	US-			
	M	US-			

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*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Sathi Perumal ("Pipelined 50 MHz CMOS ASIC for 32 bit Binary to residue conversion and residue to binary conversion" 1994).
	V	Blum T. Paar ("Montgomery modular exponentiation on reconfigurable hardware", 1999)
	W	Jia-Lin Sheu ("A pipelined architecture of fast modular multiplication for RSA cryptography", 1998)
	X	Jean-Claude Bajard ("An RNS Montgomery Modular Multiplication Algorithm", 1998)

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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	W	M. Shand ("Fast Implementations of RSA Cryptography", 1993)
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